

FEATURES

- Four 8-bit DACs in one package
- +3 V, +5 V, and ± 5 V operation
- Rail-to-rail REF input to voltage output swing
- 2.6 MHz reference multiplying bandwidth
- Internal power-on reset
- SPI serial interface-compatible—AD7304
- Fast parallel interface—AD7305
- 40 μ A power shutdown

APPLICATIONS

- Automotive output span voltage
- Instrumentation, digitally controlled calibration
- Pin-compatible AD7226 replacement when $V_{DD} < 5.5$ V

GENERAL DESCRIPTION

The AD7304/AD7305¹ are quad, 8-bit DACs that operate from a single +3 V to +5 V supply, or ± 5 V supplies. The AD7304 has a serial interface, while the AD7305 has a parallel interface. Internal precision buffers swing rail-to-rail. The reference input range includes both supply rails, allowing for positive or negative full-scale output voltages. Operation is guaranteed over the supply voltage range of 2.7 V to 5.5 V, consuming less than 9 mW from a 3 V supply.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail V_{REF} input to DAC V_{OUT} allows for a full-scale voltage set equal to the positive supply, V_{DD} , the negative supply, V_{SS} , or any value in between.

The AD7304's doubled-buffered serial data interface offers high speed, 3-wire, SPI[®], and microcontroller-compatible inputs using data in (SDI), clock (CLK), and chip select (\overline{CS}) pins. Additionally, an internal power-on reset sets the output to zero scale.

The parallel input AD7305 uses a standard address decode along with the \overline{WR} control line to load data into the input registers.

The double-buffered architecture allows all four input registers to be preloaded with new values, followed by an \overline{LDAC} control strobe that copies all the new data into the DAC registers, thereby updating the analog output values.

¹ Protected under Patent No. 5684481.

Rev. C

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FUNCTIONAL BLOCK DIAGRAMS



Figure 1.



Figure 2.

When operating from less than 5.5 V, the AD7305 is pin-compatible with the popular industry-standard AD7226.

An internal power-on reset places both parts in the zero-scale state at turn-on. A 40 μ A power shutdown (SHDN) feature is activated on both parts by three-stating the SDI/SHDN pin on the AD7304 and three-stating the A0/SHDN address pin on the AD7305.

The AD7304/AD7305 are specified over the extended industrial -40°C to $+85^{\circ}\text{C}$ and the automotive -40°C to $+125^{\circ}\text{C}$ temperature ranges. AD7304s are available in a wide-body 16-lead SOIC (R-16) package. The parallel input AD7305 is available in the wide-body 20-lead SOIC (R-20) surface-mount package. For ultracompact applications, the thin 1.1 mm, 16-lead TSSOP (RU-16) package is available for the AD7304, while the 20-lead TSSOP (RU-20) houses the AD7305.

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Revision History

11/04—Data Sheet Changed from Rev. B to Rev. C

| | |
|----------------------------------|-----------|
| Update Format | Universal |
| Update Features | 1 |
| Changes to Figure 35..... | 15 |
| Add Power-Up Sequence..... | 15 |
| Changes to Figure 36..... | 16 |
| Change to Figure 37 | 16 |
| Updated Outline Dimensions | 18 |

2/04—Data Sheet Changed from Rev. A to Rev. B

| | |
|--|-----------|
| Renumber TPCs and Figures | Universal |
| Deleted N-16 and N-20 packages..... | Universal |
| Changes to Absolute Maximum Ratings..... | 3 |
| Changes to Ordering Guide | 4 |
| Updated Outline Dimensions | 14 |

3/98—Changed from Rev. 0 to Rev. A

2/98—Revision 0: Initial Version

SPECIFICATIONS

@ $V_{DD} = 3\text{ V}$ or 5 V , $V_{SS} = 0\text{ V}$; or $V_{DD} = +5\text{ V}$ and $V_{SS} = -5\text{ V}$, $V_{SS} \leq V_{REF} \leq V_{DD}$, $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}/+125^{\circ}\text{C}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | Condition | 3 V ± 10% | 5 V ± 10% | ±5 V ± 10% | Unit |
|---|-------------------|--|-----------------|-----------------|-----------------|-------------------------|
| STATIC PERFORMANCE | | | | | | |
| Resolution ¹ | N | | 8 | 8 | 8 | Bits |
| Integral Nonlinearity ² | INL | | ±1 | ±1 | ±1 | LSB max |
| Differential Nonlinearity | DNL | Monotonic, all codes 0 to 0xFF | ±1 | ±1 | ±1 | LSB max |
| Zero-Scale Error | V_{ZSE} | Data = 0x00 | 15 | 15 | ±15 | mV max |
| Full-Scale Voltage Error | V_{FSE} | Data = 0xFF | ±4 | ±4 | ±4 | LSB max |
| Full-Scale Temperature Coefficient ³ | TCV_{FS} | | 5 | 5 | 5 | ppm/°C typ ⁴ |
| REFERENCE INPUT | | | | | | |
| V_{REFIN} Range | V_{REFIN} | | V_{SS}/V_{DD} | V_{SS}/V_{DD} | V_{SS}/V_{DD} | V min/max |
| Input Resistance (AD7304) | R_{REFIN} | Code = 0x55 | 28 | 28 | 28 | kΩ typ |
| Input Resistance (AD7305) | R_{REFIN} | All DACs at code = 0x55 | 7.5 | 7.5 | 7.5 | kΩ typ |
| Input Capacitance ³ | C_{REFIN} | | 5 | 5 | 5 | pF typ |
| ANALOG OUTPUTS | | | | | | |
| Output Voltage Range | V_{OUT} | | V_{SS}/V_{DD} | V_{SS}/V_{DD} | V_{SS}/V_{DD} | V min/max |
| Output Current Drive | I_{OUT} | Code = 0x80, $\Delta V_{OUT} < 1\text{ LSB}$ | ±3 | ±3 | ±3 | mA typ |
| Shutdown Resistance | R_{OUT} | DAC outputs placed in shutdown state | 120 | 120 | 120 | kΩ typ |
| Capacitive Load ³ | C_L | No oscillation | 200 | 200 | 200 | pF typ |
| LOGIC INPUTS | | | | | | |
| Logic Input Low Voltage | V_{IL} | | 0.6 | 0.8 | 0.8 | V min |
| Logic Input High Voltage | V_{IH} | | 2.1 | 2.4 | 2.4 | V max |
| Input Leakage Current ⁵ | I_{IL} | | ±10 | ±10 | ±10 | μA max |
| Input Capacitance ³ | C_{IL} | | 8 | 8 | 8 | pF max |
| AC CHARACTERISTICS³ | | | | | | |
| Output Slew Rate | SR | Code = 0x00 to 0xFF to 0x00 | 1/2.7 | 1/3.6 | 1.0/3.6 | V/μs min/typ |
| Reference Multiplying | BW | Small signal, $V_{SS} = -5\text{ V}$ | | | 2.6 | MHz typ |
| Total Harmonic Distortion | THD | $V_{REF} = 4\text{ V p-p}$, $V_{SS} = -5\text{ V}$, $f = 1\text{ kHz}$ | | | 0.025 | % |
| Settling Time ⁶ | t_s | To ±0.1% of full scale | 1.1/2 | 1.0/2 | 1.0/2 | μs typ/max |
| Shutdown Recovery Time | t_{SDR} | To ±0.1% of full scale | 2 | 2 | 2 | μs max |
| Time to Shutdown | t_{SDN} | | 15 | 15 | 15 | μs typ |
| DAC Glitch | Q | | 15 | 15 | 15 | nVs typ |
| Digital Feedthrough | Q | | 2 | 2 | 2 | nVs typ |
| Feedthrough | V_{OUT}/V_{REF} | Code = 0x00, $V_{REF} = 1\text{ V p-p}$, $f = 100\text{ kHz}$ | | | -65 | dB |
| SUPPLY CHARACTERISTICS | | | | | | |
| Positive Supply Current | I_{DD} | $V_{LOGIC} = 0\text{ V}$ or V_{DD} , no load | 6 | 6 | 6 | mA max |
| Negative Supply Current | I_{SS} | $V_{SS} = -5\text{ V}$ | | | 6 | mA max |
| Power Dissipation | P_{DISS} | $V_{LOGIC} = 0\text{ V}$ or V_{DD} , no load | 15 | 30 | 60 | mW max |
| Power Down | I_{DD_SD} | SDI/SHDN = floating | 40 | 40 | 40 | μA typ |
| Power Supply Sensitivity | PSS | $\Delta V_{DD} = \pm 10\%$ | 0.004 | 0.004 | 0.004 | %/% |

¹ One LSB = $V_{REF}/256$.

² The first three codes (0x00, 0x01, 0x10) are excluded from the integral nonlinearity error measurement in single-supply operation 3 V or 5 V.

³ These parameters are guaranteed by design and not subject to production testing.

⁴ Typical specifications represent average readings measured at 25°C.

⁵ The SDI/SHDN and A0/SHDN pins have a 30 μA maximum I_{IL} input leakage current.

⁶ The settling time specification does not apply for negative going transitions within the last three LSBs of ground in single-supply operation.



Figure 3. Rail-to-Rail Reference Input to Output at 20 kHz

TIMING SPECIFICATIONS

@ $V_{DD} = 3\text{ V}$ or 5 V , $V_{SS} = 0\text{ V}$; or $V_{DD} = +5\text{ V}$ and $V_{SS} = -5\text{ V}$, $V_{SS} \leq V_{REF} \leq V_{DD}$, $-40^\circ\text{C} < T_A < +85^\circ\text{C}/+125^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | 3 V ± 10% | 5 V ± 10% | ±5 V ± 10% | Unit |
|--|------------|-----------|-----------|------------|--------|
| INTERFACE TIMING SPECIFICATIONS ^{1,2} | | | | | |
| AD7304 Only | | | | | |
| Clock Width High | t_{CH} | 70 | 55 | 55 | ns min |
| Clock Width Low | t_{CL} | 70 | 55 | 55 | ns min |
| Data Setup | t_{DS} | 50 | 40 | 40 | ns min |
| Data Hold | t_{DH} | 30 | 20 | 20 | ns min |
| Load Pulse Width | t_{LDW} | 70 | 60 | 60 | ns min |
| Load Setup | t_{LD1} | 40 | 30 | 30 | ns min |
| Load Hold | t_{LD2} | 40 | 30 | 30 | ns min |
| Clear Pulse Width | t_{CLWR} | 60 | 60 | 60 | ns min |
| Select | t_{CSS} | 30 | 20 | 20 | ns min |
| Deselect | t_{CSH} | 60 | 40 | 40 | ns min |
| AD7305 Only | | | | | |
| Data Setup | t_{DS} | 60 | 40 | 40 | ns min |
| Data Hold | t_{DH} | 30 | 20 | 20 | ns min |
| Address Setup | t_{AS} | 60 | 40 | 40 | ns min |
| Address Hold | t_{AH} | 30 | 20 | 20 | ns min |
| Write Width | t_{WR} | 60 | 50 | 50 | ns min |
| Load Pulse Width | t_{LDW} | 60 | 50 | 50 | ns min |
| Load Setup | t_{LS} | 60 | 40 | 40 | ns min |
| Load Hold | t_{LH} | 30 | 20 | 20 | ns min |

¹ These parameters are guaranteed by design and not subject to production testing.

² All input control signals are specified with $t_r = t_f = 2\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--|--|
| V _{DD} to GND | −0.3 V, +8 V |
| V _{SS} to GND | +0.3 V, −8 V |
| V _{REFX} to GND | V _{SS} , V _{DD} |
| Logic Inputs to GND | −0.3 V, V _{DD} + 0.3 V |
| V _{OUTX} to GND | −0.3 V, V _{DD} + 0.3 V |
| I _{OUT} Short-Circuit to GND | 50 mA |
| Package Power Dissipation | (T _{J MAX} − T _A)/θ _{JA} |
| Thermal Resistance θ _{JA} | |
| 16-Lead SOIC Package (R-16) | 73°C/W |
| 16-Lead TSSOP Package (RU-16) | 180°C/W |
| 20-Lead SOIC Package (R-20) | 74°C/W |
| 20-Lead TSSOP Package (RU-20) | 155°C/W |
| Maximum Junction Temperature (T _{J MAX}) | 150°C |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature | |
| R-16, R-20, RU-16, RU-20 (Vapor Phase, 60 sec) | 235°C |
| R-16, R-20, RU-16, RU-20 (Infrared, 15 sec) | 220°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD7304/AD7305

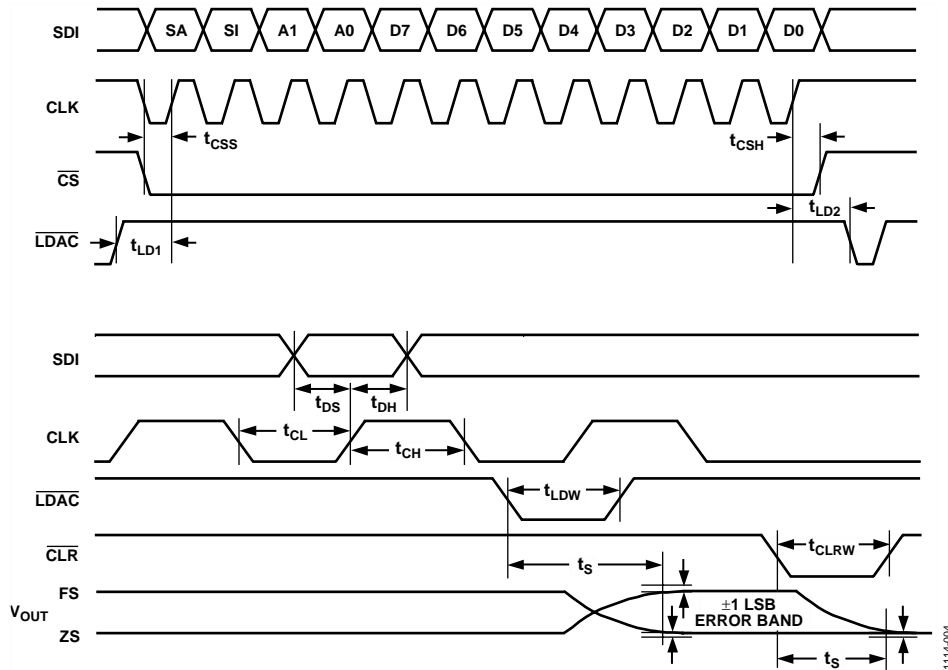


Figure 4. AD7304 General Timing Diagram

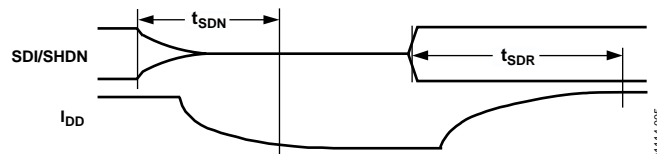


Figure 5. AD7304 Timing Diagram Zoom In

Table 4. AD7304 Control Logic Truth Table

| CS ¹ | CLK ¹ | LDAC | CLR ¹ | Serial Shift Register Function | Input REG Function | DAC Register Function |
|-----------------|------------------|------|------------------|--------------------------------|---------------------------------------|--|
| H | X | H | H | No effect | No effect | No effect |
| L | ↑+ | H | H | Data advanced 1 bit | No effect | No effect |
| ↑+ | L | H | H | No effect | Updated with SR contents ² | No effect |
| H | X | L | H | No effect | Latched with SR contents ² | All input register contents transferred ³ |
| H | X | H | ↓- | No effect | Loaded with 0x00 | Loaded with 0x00 |
| H | X | H | ↑+ | No effect | Latched with 0x00 | Latched with 0x00 |

¹ ↑+ positive logic transition; ↓- negative logic transition; X Don't Care.

² One input register receives the data bits D7–D0 decoded from the SR address bits (A1, A0), where REG A = (0, 0), B = (0, 1), C = (1, 0), and D = (1, 1).

³ LDAC is a level-sensitive input.

Table 5. AD7304 Serial Input Register Data Format, Data is Loaded in MSB-First Format

| | MSB B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | LSB B0 |
|--------|------------|-----|----|----|----|----|----|----|----|----|----|-----------|
| AD7304 | SAC | SDC | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

If B11 (SAC), *Shutdown All Channels*, is set to logic low, all DACs are placed in a power shutdown mode, and all output voltages become high resistance. If B10 (SDC), *Shutdown Decoded Channel*, is set to logic low, only the DAC decoded by Address Bits A1 and A0 is placed in shutdown mode.

Table 6. AD7305 Control Logic Truth Table

| WR ¹ | A1 | A0 | LDAC ² | Input Register Function | DAC Register Function |
|-----------------|----|----|-------------------|--|--|
| L | L | L | H | Register A loaded with DB0 to DB7 | Latched with previous contents, no change |
| ↑+ | L | L | H | Register A latched with DB0 to DB7 | Latched with previous contents, no change |
| L | L | H | H | Register B loaded with DB0 to DB7 | Latched with previous contents, no change |
| ↑+ | L | H | H | Register B latched with DB0 to DB7 | Latched with previous contents, no change |
| L | H | L | H | Register C loaded with DB0 to DB7 | Latched with previous contents, no change |
| ↑+ | H | L | H | Register C latched with DB0 to DB7 | Latched with previous contents, no change |
| L | H | H | H | Register D loaded with DB0 to DB7 | Latched with previous contents, no change |
| ↑+ | H | H | H | Register D latched with DB0 to DB7 | Latched with previous contents, no change |
| H | X | X | L | No effect | All input register contents loaded, register transparent |
| L | X | X | L | Input register x transparent to DB0 to DB7 | Register transparent |
| H | X | X | ↑+ | No effect | All input register contents latched |
| H | X | X | H | No effect, device not selected | No effect, device not selected |

¹ ↑+ positive logic transition; ↓- negative logic transition; X don't care.
² LDAC is a level-sensitive input.

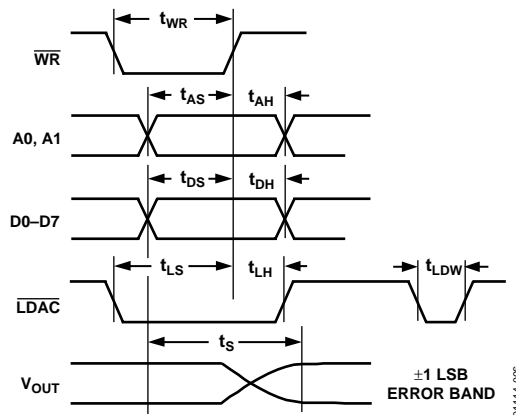


Figure 6. AD7305 General Timing Diagram

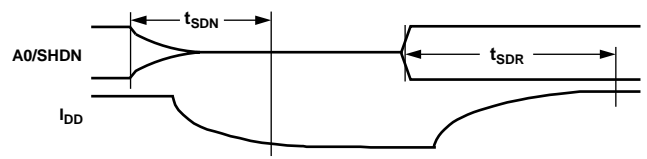


Figure 7. AD7305 Timing Diagram Zoom In

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

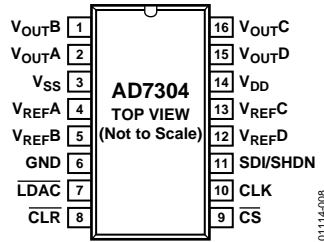


Figure 8. AD7304 Pin Configuration

Table 7. AD7304 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|---|
| 1 | V _{OUTB} | Channel B Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFB} pin. Output is open circuit when SHDN is enabled. |
| 2 | V _{OUTA} | Channel A Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFA} pin. Output is open circuit when SHDN is enabled. |
| 3 | V _{SS} | Negative Power Supply Input. Specified range of operation is 0 V to –5.5 V. |
| 4 | V _{REFA} | Channel A Reference Input. Establishes V _{OUTA} full-scale voltage. Specified range of operation is V _{SS} < V _{REFA} < V _{DD} . |
| 5 | V _{REFB} | Channel B Reference Input. Establishes V _{OUTB} full-scale voltage. Specified range of operation is V _{SS} < V _{REFB} < V _{DD} . |
| 6 | GND | Common Analog and Digital Ground. |
| 7 | LDAC | Load DAC Register Strobe, Active Low. Simultaneously transfers data from all four input registers into the corresponding DAC registers. Asynchronous active low input. DAC register is transparent when LDAC = 0. See Table 4 for operation. |
| 8 | CLR | Clears All Input and DAC Registers to the Zero Condition. Asynchronous active low input. The serial register is not effected. |
| 9 | CS | Chip Select, Active Low Input. Disables shift register loading when high. Transfers serial input register data to the decoded input register when CS returns high. Does not effect LDAC operation. |
| 10 | CLK | Clock Input, Positive Edge Clocks Data into Shift Register. Disabled by chip select CS. |
| 11 | SDI/SHDN | Serial Data Input Loads Directly into the Shift Register, MSB First. Hardware shutdown (SHDN) control input, active when pin is left floating by a three-state logic driver. Does not effect DAC register contents as long as power is present on V _{DD} . |
| 12 | V _{REFD} | Channel D Reference Input. Establishes V _{OUTD} full-scale voltage. Specified range of operation is V _{SS} < V _{REFD} < V _{DD} . |
| 13 | V _{REFC} | Channel C Reference Input. Establishes V _{OUTC} full-scale voltage. Specified range of operation is V _{SS} < V _{REFC} < V _{DD} . |
| 14 | V _{DD} | Positive Power Supply Input. Specified range of operation is 2.7 V to 5.5 V. |
| 15 | V _{OUTD} | Channel D Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFD} pin. Output is open circuit when SHDN is enabled. |
| 16 | V _{OUTC} | Channel C Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFC} pin. Output is open circuit when SHDN is enabled. |



Figure 9. AD7305 Pin Configuration

Table 8. AD7305 Pin Function Description

| Pin No. | Mnemonic | Description |
|---------|-------------------|--|
| 1 | V _{OUTB} | Channel B Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFB} pin. Output is open circuit when SHDN is enabled. |
| 2 | V _{OUTA} | Channel A Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFA} pin. Output is open circuit when SHDN is enabled. |
| 3 | V _{SS} | Negative Power Supply Input. Specified range of operation is 0 V to –5.5 V. |
| 4 | V _{REF} | Channel B Reference Input. Establishes V _{OUT} full-scale voltage. Specified range of operation is V _{SS} < V _{REF} < V _{DD} . |
| 5 | GND | Common Analog and Digital Ground. |
| 6 | LDAC | Load DAC Register Strobe, Active Low. Simultaneously transfers data from all four input registers into the corresponding DAC registers. Asynchronous active low input. DAC register is transparent when LDAC = 0. See Table 6 for operation. |
| 7 | DB7 | MSB Digital Input Data Bit. |
| 8 | DB6 | Data Bit 6. |
| 9 | DB5 | Data Bit 5. |
| 10 | DB4 | Data Bit 4. |
| 11 | DB3 | Data Bit 3. |
| 12 | DB2 | Data Bit 2. |
| 13 | DB1 | Data Bit 1. |
| 14 | DB0 | LSB Digital Input Data Bit. |
| 15 | WR | Write Data into Input Register Control Line, Active Low. See Table 6 for operation. |
| 16 | A1 | Address Bit 1. |
| 17 | A0/SHDN | Address Bit 0/Hardware Shutdown (SHDN) Control Input, Active When Pin Is Left Floating by a Three-State Logic Driver. Does not effect DAC register contents as long as power is present on V _{DD} . |
| 18 | V _{DD} | Positive Power Supply Input. Specified range of operation is 2.7 V to 5.5 V. |
| 19 | V _{OUTD} | Channel D Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFD} pin. Output is open circuit when SHDN is enabled. |
| 20 | V _{OUTC} | Channel C Rail-to-Rail Buffered DAC Voltage Output. Full-scale set by reference voltage applied to V _{REFC} pin. Output is open circuit when SHDN is enabled. |

TYPICAL PERFORMANCE CHARACTERISTICS

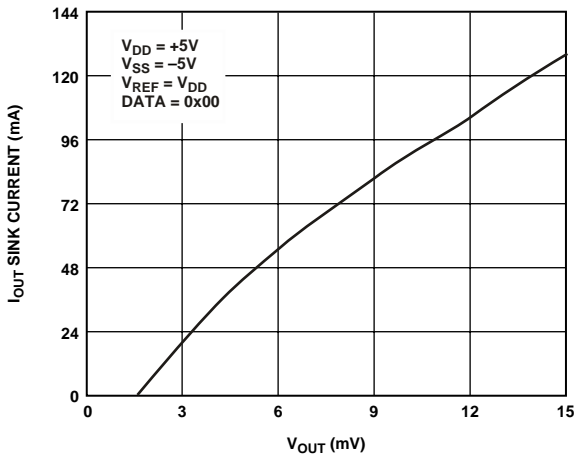


Figure 10. I_{OUT} Sink vs. V_{OUT} Rail-to-Rail Performance

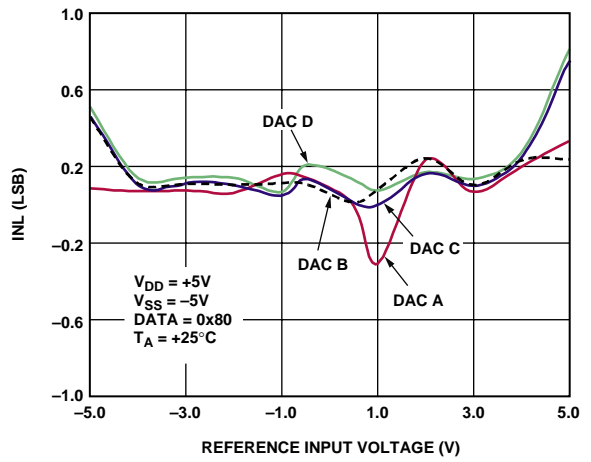


Figure 13. INL vs. Reference Input Voltage



Figure 11. I_{OUT} SOURCE vs. V_{OUT} Rail-to-Rail Performance

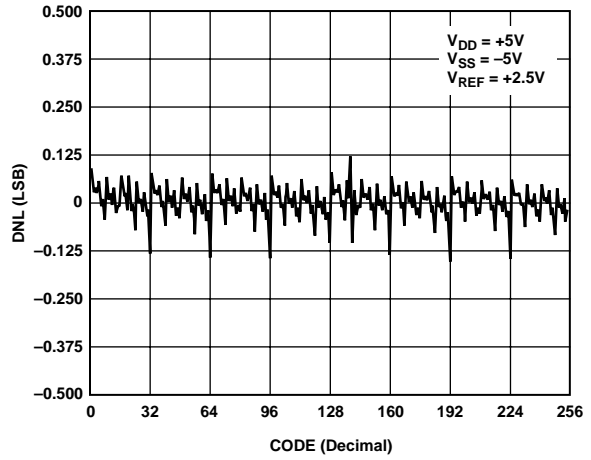


Figure 14. DNL vs. Code

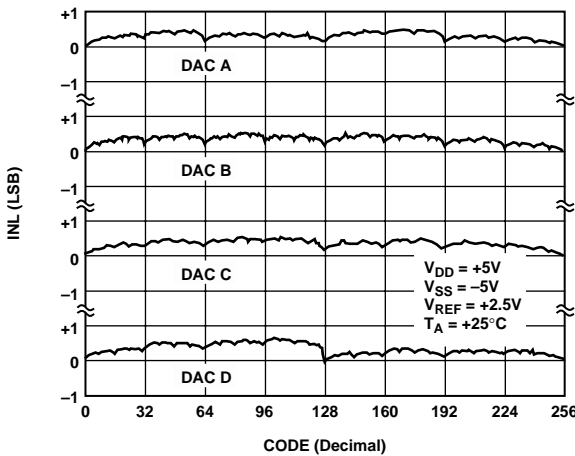


Figure 12. INL vs. Code, All DAC Channels

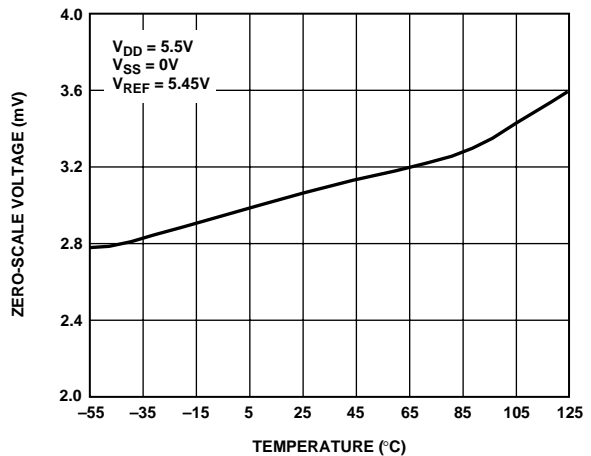


Figure 15. Zero-Scale Voltage vs. Temperature

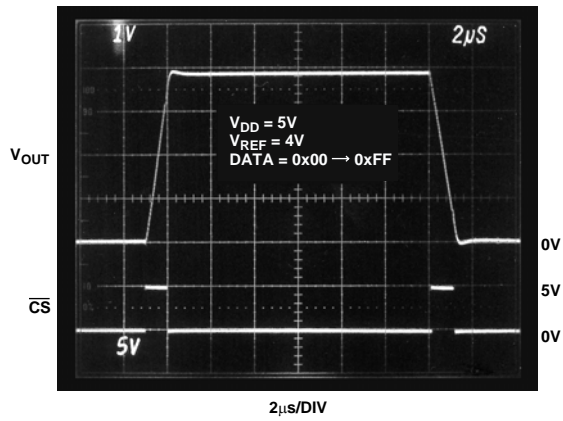


Figure 16. Large-Signal Settling Time

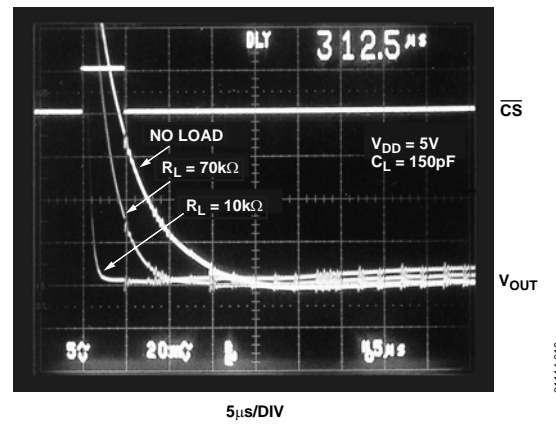


Figure 19. Time to Shutdown

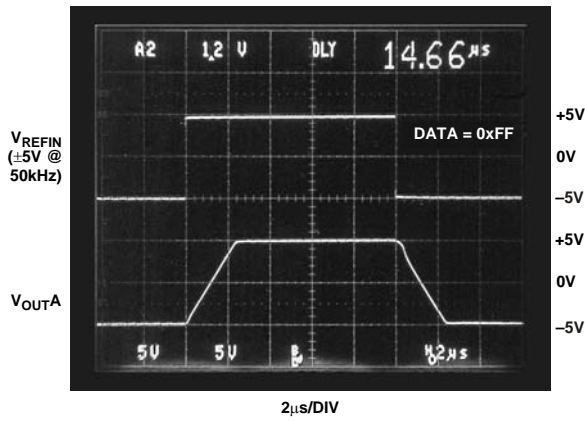


Figure 17. Multiplying Mode Step Response and Output Slew Rate

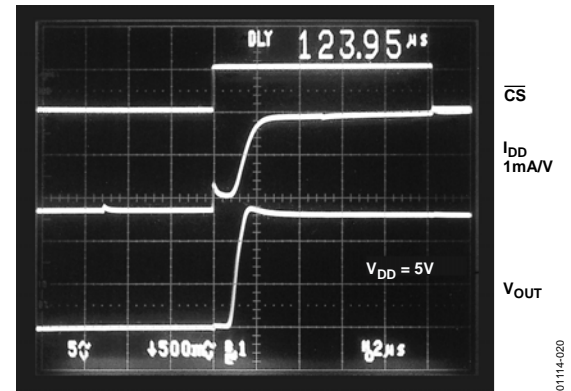


Figure 20. Shutdown Recovery Time (Wakeup)



Figure 18. Multiplying Mode Gain vs. Frequency



Figure 21. THD vs. Reference Input Amplitude

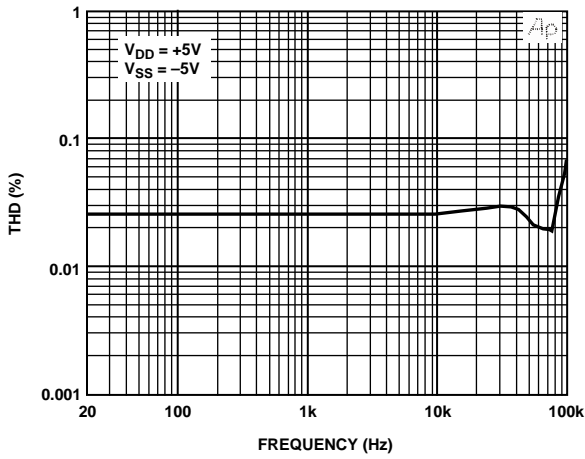


Figure 22. THD vs. Frequency

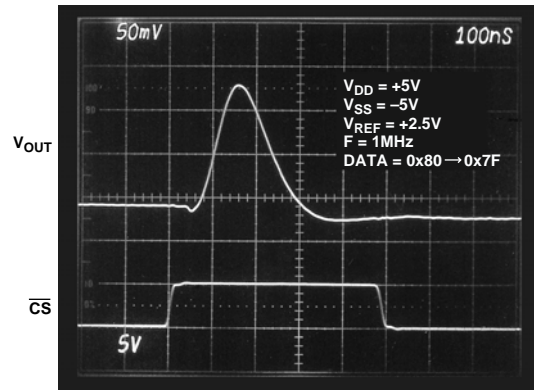


Figure 25. Midscale Transition Glitch

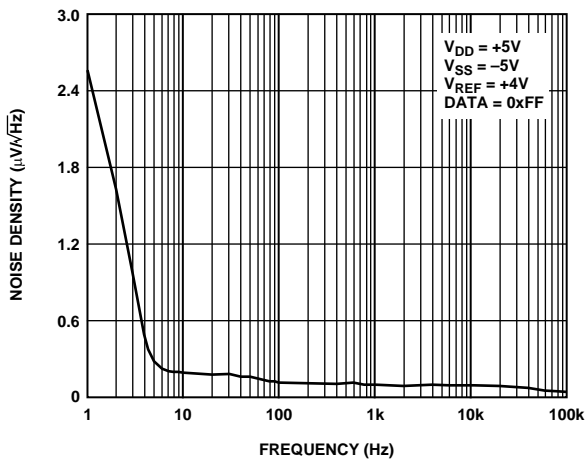


Figure 23. Output Noise Voltage Density vs. Frequency

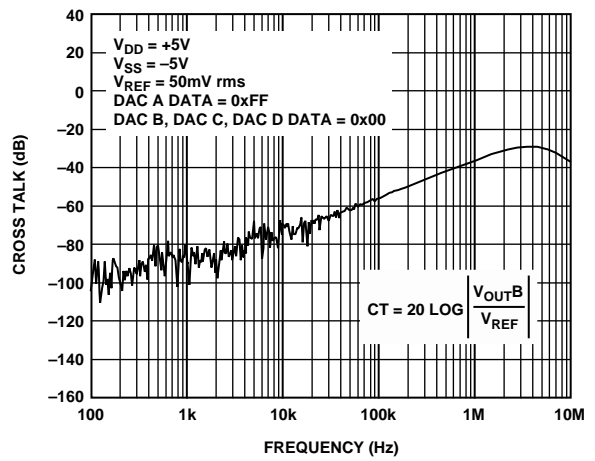


Figure 26. Crosstalk vs. Frequency



Figure 24. Digital Feedthrough



Figure 27. Power-Supply Rejection vs. Frequency



Figure 28. Supply Current vs. Digital Input Voltage



Figure 31. Shutdown Supply Current vs. Temperature

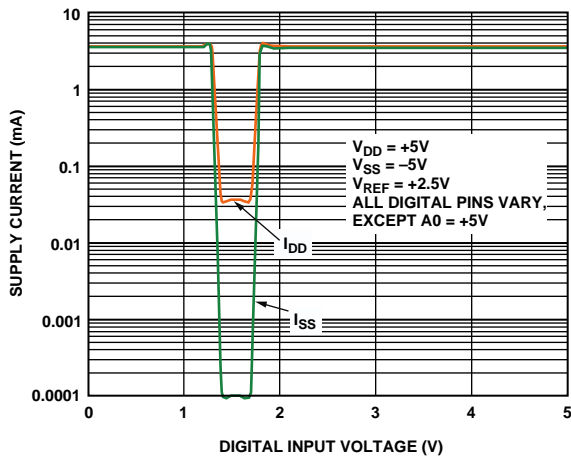


Figure 29. Shutdown Supply Current vs. Digital Input Voltage (A0 Only)



Figure 32. Normalized TUE Drift Accelerated by Burn-In Hours of Operation @ 150°C



Figure 30. Supply Current vs. Temperature

CIRCUIT OPERATION

The AD7304/AD7305 are 4-channel, 8-bit, voltage output DACs, differing primarily in digital logic interface and number of reference inputs. Both parts share the same internal DAC design and true rail-to-rail output buffers. The AD7304 contains four independent multiplying reference inputs, while the AD7305 has one common reference input. The AD7304 uses a 3-wire SPI-compatible serial data interface, while the AD7305 offers an 8-bit parallel data interface.

DAC SECTION

Each part contains four voltage-switched R-2R ladder DACs. Figure 33 shows a typical equivalent DAC. These DACs are designed to operate both single-supply or dual-supply, depending on whether the user supplies a negative voltage on the V_{SS} pin. In a single-supply application, the V_{SS} is tied to ground. In either mode, the DAC output voltage is determined by the V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register according to Equation 1.

$$V_{OUT} = V_{REF} D/256 \quad (1)$$

Note that the output full-scale polarity is the same as the V_{REF} polarity for dc reference voltages.

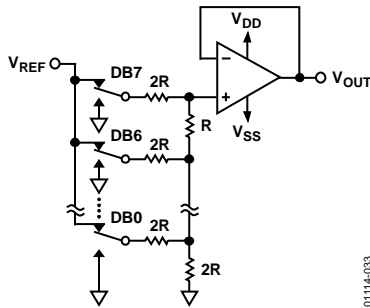


Figure 33. Typical Equivalent DAC Channel

0114-033

These DACs are also designed to accommodate ac reference input signals. As long as the ac signals are maintained between $V_{SS} < V_{REF} < V_{DD}$, the user can expect 50 kHz of full power, multiplying bandwidth performance. In order to use negative input reference voltages, the V_{SS} pin must be biased with a negative voltage of equal or greater magnitude than the reference voltage.

The reference inputs are code dependent, exhibiting worst-case minimum resistance values specified in the parametric specification table. The DAC outputs V_{OUTA} , V_{OUTB} , V_{OUTC} , and V_{OUTD} are each capable of driving 2 k Ω loads in parallel with up to 500 pF loads. Output sink current and source current are shown in Figure 10 and Figure 11, respectively. The output slew rate is nominally 3.6 V/ μ s while operating from ± 5 V supplies. The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz, 65 dB of channel-to-channel isolation exists (Figure 26). Output voltage noise is plotted in Figure 23. In order to maintain good analog performance, power supply bypassing of 0.01 μ F in parallel with 1 μ F is recommended. The true rail-to-rail capability of the AD7304/AD7305 allows the user to connect the reference inputs directly to the same supply as the V_{DD} or V_{SS} pin (Figure 34). Under these conditions, clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used.

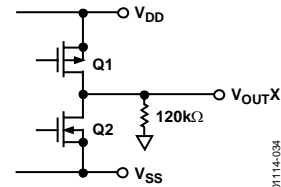


Figure 34. Equivalent DAC Amplifier Output Circuit

0114-034

AD7304 SERIAL DATA INTERFACE

The AD7304 uses a 3-wire ($\overline{\text{CS}}$, SDI, CLK) SPI-compatible serial data interface. New serial data is clocked into the serial input register in a 12-bit data-word format. MSB bits are loaded first.

Table 5 defines the 12 data-word bits. Data is placed on the SDI/SHDN pin and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Timing Specifications section. Data can only be clocked in while the $\overline{\text{CS}}$ chip select pin is active low. Only the last 12-bits clocked into the serial register are interrogated when the $\overline{\text{CS}}$ pin returns to the logic high state, extra data bits are ignored. Since most microcontrollers output serial data in 8-bit bytes, two right-justified data bytes can be written to the AD7304. Keeping the $\overline{\text{CS}}$ line low between the first and second byte transfer results in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{\text{CS}}$ initiates either the transfer of new data to the target DAC register, determined by the decoding of Address Bits A1 and A0, or the shutdown features is activated based on the SAC or SDC bits. When either SAC or SDC pins are set (Logic 0), the loading of new data determined by Bits B9 to B0 are still loaded, but the results do not appear on the buffer outputs until the device is brought out of the shutdown state. The selected DAC output voltages become high impedance with a nominal resistance of 120 k Ω to ground, see Figure 34. If both the SAC and SDC pins are set, all channels are still placed in shutdown mode. When the AD7304 has been programmed into the power shutdown state, the present DAC register data is maintained as long as V_{DD} remains greater than 2.7 V. The remaining characteristics of the software serial interface are defined by Table 4, Table 5, and Figure 5.

Two additional pins, $\overline{\text{CLR}}$ and $\overline{\text{LDAC}}$, on the AD7304 provide hardware control over the clear function and the DAC register loading. If these functions are not needed, the $\overline{\text{CLR}}$ pin can be tied to logic high, and the $\overline{\text{LDAC}}$ pin can be tied to logic low. The asynchronous input $\overline{\text{CLR}}$ pin forces all input and DAC registers to the zero-code state. The asynchronous $\overline{\text{LDAC}}$ pin can be strobed to active low when all DAC registers need to be updated simultaneously from their respective input registers.

The $\overline{\text{LDAC}}$ pin places the DAC register in a transparent mode while in the logic low state.



Figure 35. AD7304 Equivalent Logic Interface

AD7304 HARDWARE SHUTDOWN SHDN

If a three-state driver is used on the SDI/SHDN pin, the AD7304 can be placed into a power shutdown mode when the SDI/SHDN pin is placed in a high impedance state. For proper operation, no other termination voltages should be present on this pin. An internal window comparator detects when the logic voltage on the SHDN pin is between 28% and 36% of V_{DD} . A high impedance internal bias generator provides this voltage on the SHDN pin. The four DAC output voltages become high impedance with a nominal resistance of 120 k Ω to ground (see Figure 34 for an equivalent circuit).

AD7304/AD7305 POWER-ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the input and DAC registers to the zero-code state. The V_{DD} power supply should have a monotonically increasing ramp in order to have consistent results, especially in the region of $V_{\text{DD}} = 1.5 \text{ V}$ to 2.3 V. The V_{SS} supply has no effect on the power-on reset performance. The DAC register data stays at zero until a valid serial register software load takes place. In the case of the double-buffered AD7305, the output DAC register can only be changed once the $\overline{\text{LDAC}}$ strobe is initiated.

POWER-UP SEQUENCE

It is recommended to power $V_{\text{DD}}/V_{\text{SS}}$ first before applying any voltage to the reference terminals to avoid potential latch up. The ideal power-up sequence is in the following order: GND, V_{DD} , V_{SS} , Digital Inputs, and V_{REFx} . The order of powering digital inputs and reference inputs is not important as long as they are powered after $V_{\text{DD}}/V_{\text{SS}}$.

AD7304/AD7305

AD7305 PARALLEL DATA INTERFACE

The AD7305 has an 8-bit parallel interface DB7 = MSB, DB0 = LSB. Two address bits, A1 and A0, are decoded when an active low write strobe is placed on the \overline{WR} pin, see Table 6. The \overline{WR} is a level-sensitive input pin, therefore, the data setup and data hold times defined in the Timing Specifications section need to be adhered to.

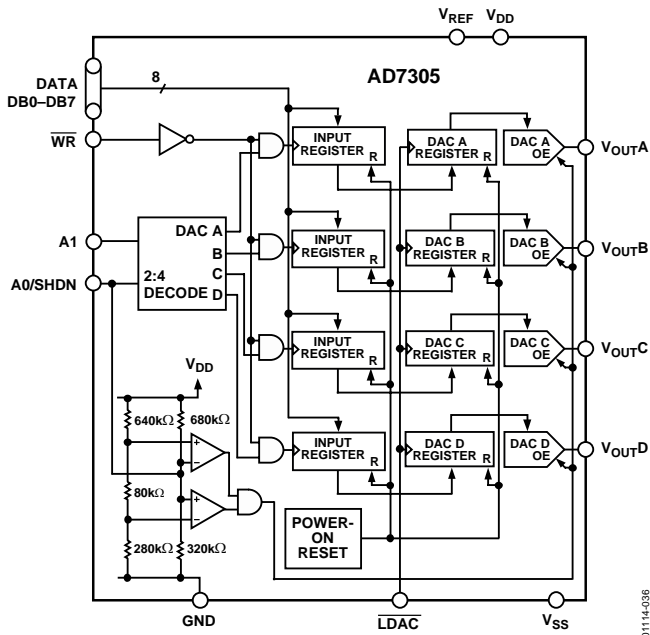


Figure 36. AD7305 Equivalent Logic Interface

The \overline{LDAC} pin provides the capability of simultaneously updating all DAC registers with new data from the input registers at the same time. This results in the analog outputs all changing to their new values at the same time. The \overline{LDAC} pin is a level-sensitive input. If the simultaneous update feature is not required, the \overline{LDAC} pin can be tied to logic low. When the

\overline{LDAC} is tied to Logic Low, the DAC registers become transparent and the input register data determines the DAC output voltage (see Figure 36 for an equivalent interface logic diagram).

AD7226 PIN COMPATIBILITY

By tying the \overline{LDAC} pin to ground, the AD7305 has the same pin configuration and functionality as the AD7226, with the exception of a lower power supply operating voltage.

AD7305 HARDWARE SHUTDOWN SHDN

If a three-state driver is used on the A0/SHDN pin, the AD7305 can be placed into a power shutdown mode when the A0/SHDN pin is placed in a high impedance state. For proper operation, no other termination voltages should be present on this pin. An internal window comparator detects when the logic voltage on the SHDN pin is between 28% and 36% of V_{DD} . A high impedance, internal-bias generator provides this voltage on the SHDN pin. The four DAC output voltages become high impedance with a nominal resistance of 120 kΩ to ground.

ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zeners connected to ground (GND). The V_{REF} pins also contain a back-biased ESD protection Zener connected to V_{DD} (see Figure 37).



Figure 37. Equivalent ESD Protection Circuits

APPLICATIONS

The AD7304/AD7305 are inherently 2-quadrant multiplying DACs. That is, they can easily be set up for unipolar output operation. The full-scale output polarity is the same as the reference input voltage polarity.

In some applications, it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished using an external true rail-to-rail op amp, such as the OP295. Connecting the external amplifier with two equal value resistors, as shown in Figure 38, results in a full 4-quadrant multiplying circuit. In this circuit, the amplifier provides a gain of two, which increases the output span magnitude to 10 V. The transfer equation of this circuit shows that both negative and positive output voltages are created as

the input data (D) is incremented from code zero ($V_{OUT} = -5\text{ V}$) to midscale ($V_{OUT} = 0\text{ V}$) to full scale ($V_{OUT} = +5\text{ V}$).

$$V_{OUT} = \frac{D}{128-1} \times V_{REF} \quad (2)$$



Figure 38. 4-Quadrant Multiplying Application Circuit

01114-038

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 39. 16-Lead Standard Small Outline Package [SOIC]
 Wide Body (R-16)
 Dimensions shown in millimeters and (inches)



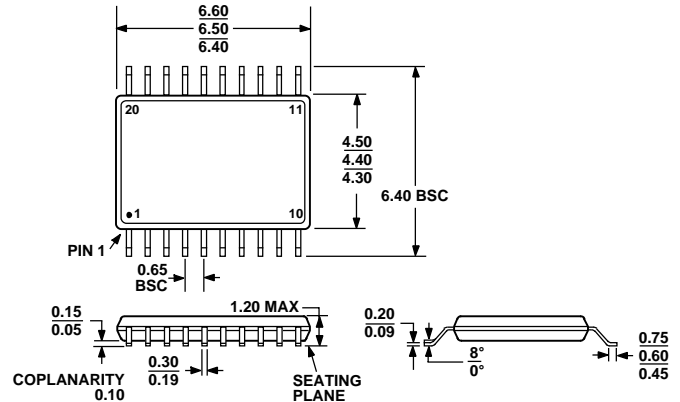
COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 41. 16-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-16)
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-013AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 40. 20-Lead Standard Small Outline Package [SOIC]
 Wide Body (R-20)
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153AC

Figure 42. 20-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-20)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Options |
|-------------------------------|--------------------------|----------------------------|------------------------|
| AD7304BR | -40°C to +85°C | 16-Lead SOIC | R-16 |
| AD7304BR-REEL | -40°C to +85°C | 16-Lead SOIC | R-16 |
| AD7304BRZ ¹ | -40°C to +85°C | 16-Lead SOIC | R-16 |
| AD7304BRZ-REEL ¹ | -40°C to +85°C | 16-Lead SOIC | R-16 |
| AD7304YR | -40°C to +125°C | 16-Lead SOIC | R-16 |
| AD7304YRZ ¹ | -40°C to +125°C | 16-Lead SOIC | R-16 |
| AD7304BRU | -40°C to +85°C | 16-Lead TSSOP | RU-16 |
| AD7304BRU-REEL7 | -40°C to +85°C | 16-Lead TSSOP | RU-16 |
| AD7305BR | -40°C to +85°C | 20-Lead SOIC | R-20 |
| AD7305BR-REEL | -40°C to +85°C | 20-Lead SOIC | R-20 |
| AD7305YR | -40°C to +125°C | 20-Lead SOIC | R-20 |
| AD7305YR-REEL | -40°C to +125°C | 20-Lead SOIC | R-20 |
| AD7305BRU | -40°C to +85°C | 20-Lead TSSOP | RU-20 |
| AD7305BRU-REEL7 | -40°C to +85°C | 20-Lead TSSOP | RU-20 |
| AD7305BRUZ ¹ | -40°C to +85°C | 20-Lead TSSOP | RU-20 |
| AD7305BRUZ-REEL7 ¹ | -40°C to +85°C | 20-Lead TSSOP | RU-20 |

¹ Z = Pb-free part.

NOTES